A Digital Pixel Sensor with 0.17%/-0.32% Non-Linearity and 75.3μW Power Consumption Using Wide-Swing PWM and Embedded 10-bit 3T-GC-eDRAM

Cheng-Jhe Li, Guan-Cheng Chen, and Chih-Cheng Hsieh, *Senior Member, IEEE*
National Tsing Hua University, Hsinchu, Taiwan

***Abstract*— This paper introduces a digital pixel sensor (DPS) using wide-swing pulse-width modulation (PWM) with high linearity, low power consumption, and embedded 10-bit pixel-level storage units. The photo-generated signal, after exposure, is converted into a corresponding pulse width using PWM operation, which then latches the code from a global counter and stores it in the embedded 10-bit memory. This process enables parallel analog-to-digital conversion within the pixel array, thereby reducing noise and improving signal fidelity. The optimized embedded 3T-GC-eDRAM memory architecture, compared to 1T1C eDRAM, offers enhanced data retention and signal integrity through increased storage capacitance and amplified readout charge flow while consuming less power. The sensor is fabricated using TSMC standard 180nm 1P6M CMOS technology, with a pixel pitch of 15 μm and a total area of 2700 × 2700 μm². It operates at a supply voltage of 1.5V/1.2V and a frame rate of 181.8 fps, achieving a low non-linearity of 0.17%/-0.32%, a high linear range of 0.9V, and the imaging Figure of Merit (iFoM) of 25.3 pJ/pixel·frame.**

I. INTRODUCTION

Wireless sensor networks (WSNs) play a critical role across various domains, including the Internet of Things (IoT). Due to their ubiquity, one of the main challenges encountered by such wireless sensors is the power consumption reduction [1]. Moreover, to perform quantitative image analysis, such as shading correction, linear transformation, and flat fielding, the image sensor should exhibit a linear response [2]. A previous study [3] has shown the effectiveness of pulse width modulation (PWM) pixel operating with an ultra-low supply voltage to effectively reduce the image sensor's power consumption. However, due to the ultra-low supply voltage, the image sensor's linear range was limited. On the other hand, digital pixel sensor (DPS)-based image sensors allow illumination-to-digital conversion at the pixel level. With pixel-parallel signal conversion, DPS exhibits several advantages, such as faster parallel processing, reduced readout noise level, improved dynamic range, and better scalability with the CMOS process. Prior works have presented different in-pixel memory cells for the DPS architecture, such as counter/register [4] and SRAM [5-6]. However, implementing in-pixel memory cells in such ways occupies a significant area, resulting in a larger pixel pitch. In this work, a PWM pixel structure is presented with an improved output linear range. Moreover, a 3T-GC-eDRAM-based memory cells are utilized to improve the pixel pitch.

II. SYSTEM ARCHITECTURE

The system architecture of the proposed image sensor, as shown in Fig. 1(a), comprises a 128x128 pixel array, a global counter, and other auxiliary circuits. Each pixel is primarily composed of a photodiode (PD), a PWM circuit, and a 10-bit memory cell array, as depicted in the block diagram in Fig. 1(b). The proposed image sensor operates in a 4-phase process as shown in Fig. 1(c), consisting of "Reset", "Exposure", "Conversion" and "Readout" phases. Thanks to the DPS architecture, the "exposure" and "conversion" operations of all pixels in sensor array happen simultaneously, enabling a global shutter operation, highly-parallel PWM and analog-to-digital conversions, and in-pixel 10-bit storage. After that, the stored data can be accessed, and readout randomly or serially depends on applications. This process enhances the image quality without motion distortion and provides access flexibility with data reusability.

III. CIRCUIT IMPLEMENTATION

Fig. 2(a) shows the schematic of the pixel consisting of two main parts: the PWM circuit and the 10-bit 3T-GC-eDRAM cell array. In the PWM circuit, several techniques are employed to improve the performance, like the threshold voltage cancellation (TVC) [3] to reduce the comparator-induced fixed pattern noise (FPN), the proposed adjustable threshold voltage (ATV) to improve the V-to-T linearity of PWM operation, and the self-cutoff technique (SCT) for power reduction. Moreover, an in-pixel 10-bit memory is implemented using the 3T-GC-eDRAM due to its high memory density and long retention time.

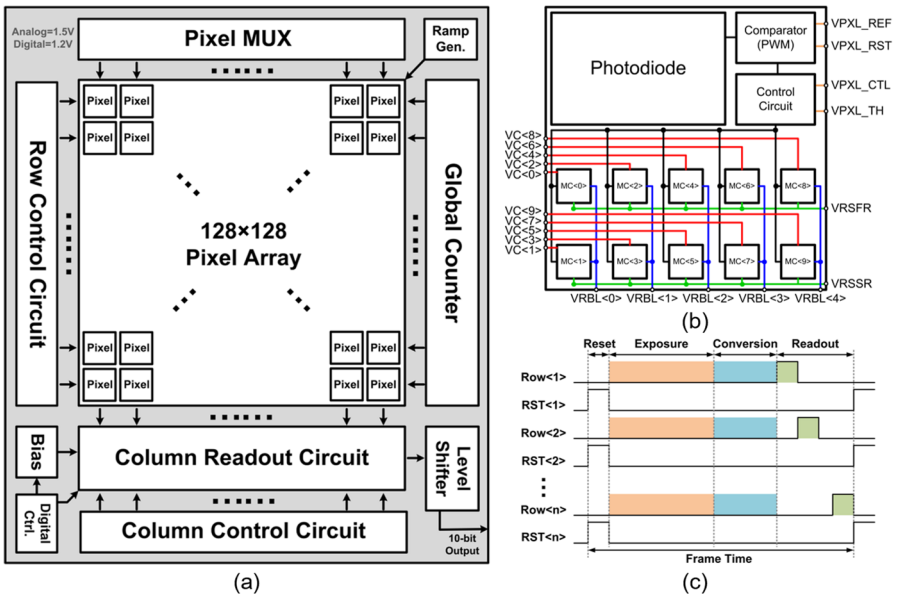


Fig. 1. (a) System architecture (b) Pixel block diagram (c) Operational timing diagram.

Fig. 2(b) illustrates the V-to-T conversion of PWM operation (ΔV_{PD}-to-V_{PW}) transition curves (in black) at different ΔV_{PD} levels with a ramping reference VPXL_REF. The transition threshold V_{SW} of the in-pixel comparator (M_{REF}/M_{PD}) for PWM operation is defined by the equality point of current between loading-PMOS (M_{REF}) and input-NMOS (M_{PD}) devices. It shows the V-to-T conversion of PWM operation keeps highly linear as long as both devices (M_{REF}/M_{PD}) remain in the saturation region at the transition point (V_{SW}), as shown in the triangular region (in green). In this work, an adjustable threshold voltage (ATV) technique is proposed to adjust the transition point (V_{SW}) from $V_{SW,CONV}$ to the optimal level $V_{SW,OPT}$ to achieve a wider ΔV_{PD} swing with high linearity using a tunable VPXL_TH and corresponding control.

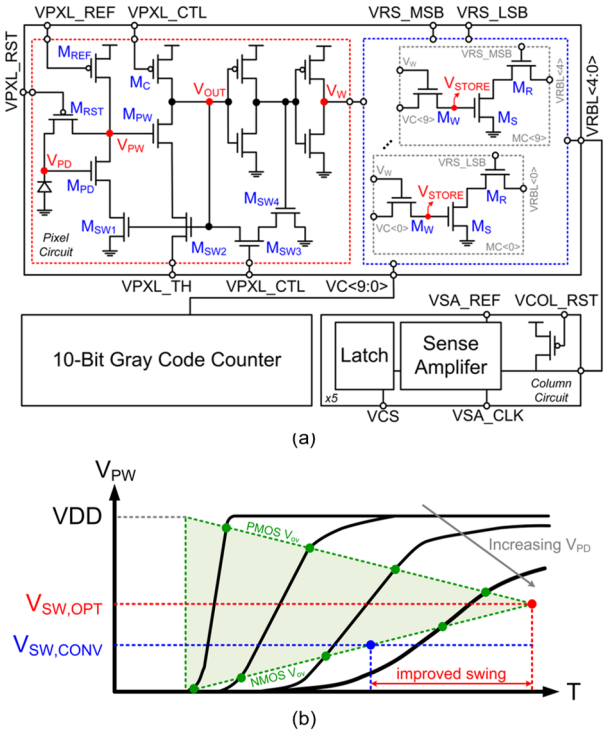


Fig. 2. (a) Pixel and readout circuit schematic (b) V-to-T conversion of PWM operation.

Fig. 3(a) illustrates the timing diagram of the proposed PWM operation in Fig. 2(a). During the reset phase, the PD is reset by turning on M_{RST}, executing the TVC reset [3]. Meanwhile, the V_{OUT} node is pre-charged to VDD through M_C. In the exposure phase, with M_{RST} turned off, the photodiode voltage (V_{PD}) decreases under illumination, resulting in an accumulated voltage difference (ΔV_{PD}) on the photodiode. During the conversion phase, a global ramp signal, VPXL_REF, is generated and applied to the gate of M_{REF} for the V-to-T conversion. Meanwhile, the transition point (V_{SW}) is adjusted to the optimal level $V_{SW,OPT}$ to achieve ATV operation for high linearity by applying a tunable reference VPXL_TH_REF. When the drain current of M_{REF} (I_M_{REF}) exceeds that of M_{PD} (I_M_{PD}), V_{PW} transitions from low to high. The feedback loop using M_{SW1}-M_{SW4}, named as the self-cutoff technique, is implemented to sense the V_{PW} transition and cut off the biasing current of I_M_{PD} for power saving.

Fig. 3(b) shows the timing diagram of the operations for parallel A-to-D conversion, in-pixel storage, and readout. During the phase for PWM and A-to-D conversions, the 10-bit digital code VC<9:0> from a global counter is generated and transmitted concurrently to the 3T-GC-eDRAM cells in each pixel. Then, the corresponding code, proportional to pulse width of PWM, is sampled and stored on V_{STORE} controlled by the buffered output V_W. After the conversion phase, the stored 10-bit data is read out controlled by VRS_MSB and VRS_LSB in an interleaved manner through a 5-bit bit-line bus VRBL<4:0> for pitch area saving. For simplicity, the readout operation of one 3T-GC-eDRAM cell is explained as an example. Firstly, the bit-line VRBL is pre-charged to VDD. Then, by turning on M_R for a fixed period of time using VRS, the discharging slope of bit-line VRBL differs depending on the stored data V_{STORE}. Enabled by VSA_CLK after a certain delay, the slope is detected using a sense amplifier with a tunable threshold (VSA_REF) for polarity judgement to enhance the readout speed. Finally, the output of the sense amplifier is latched by a column latch and sequentially read out controlled by VCS.

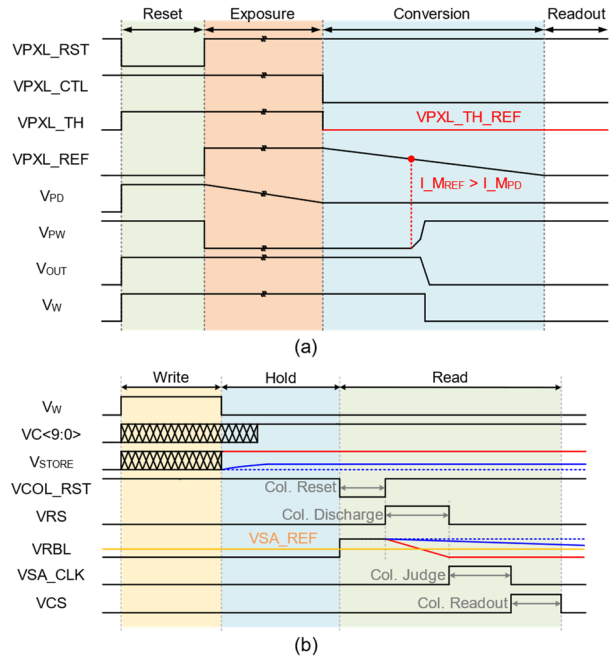


Fig. 3. The detailed timing diagram of the proposed DPS pixel.

IV. MEASUREMENT RESULTS

The prototype with a 128x128 DPS array is fabricated using TSMC standard 180nm CMOS process. Figs. 4(a)-(c) show the captured images and measured INL performance without and with the proposed ATV technique, respectively. The worst INL is improved from < 92.51 LSB (9.04%) to < 3.24 LSB (0.32%) using ATV, demonstrating a significantly better linearity and image quality.

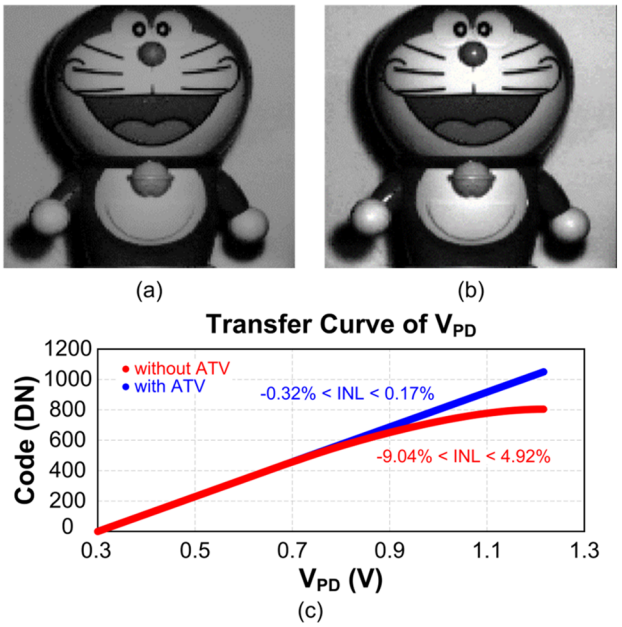


Fig. 4. The captured images (a) without ATV, (b) with ATV, (c) measured transfer curves.

Fig. 5 shows the power breakdown of a total 75.3 µW at a frame rate of 181.8 fps, which is dominated by the digital part including the counter and column readout. Thanks to the DPS architecture, the implemented pixel can operate in linear mode using exposure-then-conversion operation, as well as the high-dynamic-range (HDR) mode using exposure-while-conversion operation. Fig. 6 shows the captured images and transfer curves in both linear and HDR modes, with the achieved dynamic ranges of 52.8 dB and 80 dB, respectively.

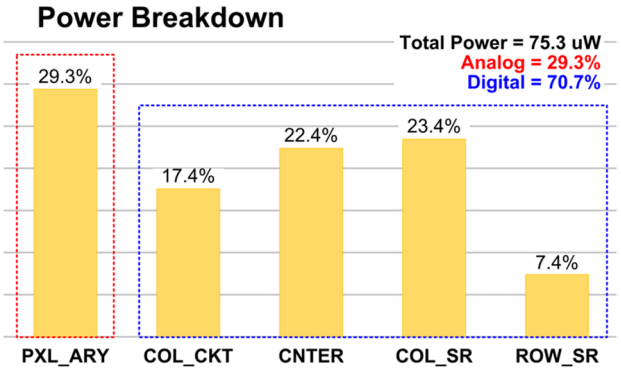


Fig. 5. The measured power breakdown

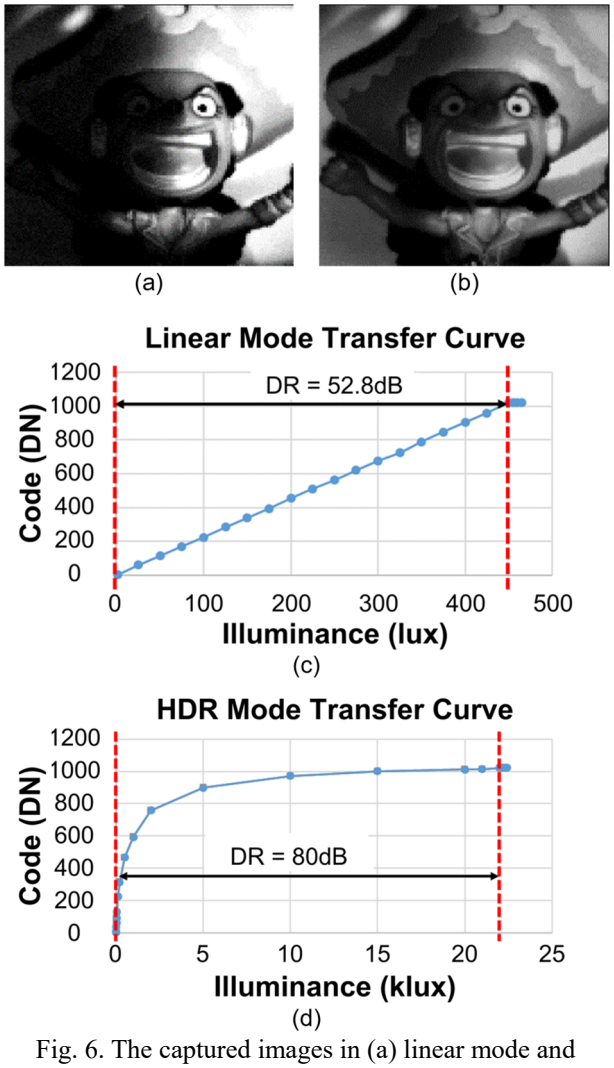


Fig. 6. The captured images in (a) linear mode and (b) HDR mode and transfer curves in (c) linear mode and (d) HDR mode.

V. CONCLUSION

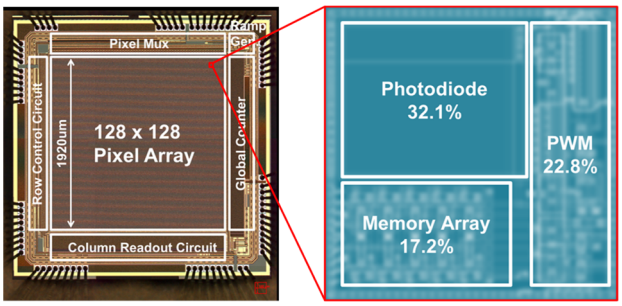
Table. 1 shows the comparison of the proposed DPS with other works. Compared to the reported PWM pixel [3], the proposed ATV achieves a larger signal swing with

Table. 1 Comparison table.

	This Work		JSSC '19 [3]	Sens. Actuators A: Phys. '15 [4]	Sens. Actuators A: Phys. '16 [5]	MVIP '22 [6]
	Linear	HDR				
CMOS technology	0.18um		0.18um	0.18um	0.18um	0.18um
Supply Voltage (V)	1.5/1.2		0.4	1	0.8	0.6
ADC (bit)	10		12	10	8	8
Memory Cell	3T-GC eDRAM		-	Counter	7T SRAM	7T SRAM
Memory Area Ratio (%)	17		-	41.7*	39.3*	59.9*
Resolution	128×128		300×200	16×16	16×16	1×1
Pixel Pitch (um)	15		7.6	23	21	18.33
Fill Factor (%)	32.1		36.2	33.5	39	24
Non-linearity	+0.17%/-0.32%	-	+0.36%/-0.29%	-	-	-
Signal Swing (V)	0.9	-	0.25	-	-	-
Dynamic Range (dB)	52.8	80	60.1	140	140	90.8**
Column FPN (%rms)(DARK)	0.05		0.07	-	-	-
Pixel FPN (%rms)(DARK)	0.43		0.16	3	3	2.93**
Frame Rate (fps)	181.8		40	-	33	33
Power(uW) (whole chip)	75.3		157	26.4	0.73	0.9**
iFoM(pJ/frame·pixel)	25.3		65*	-	85.5*	27*

(* Estimated Values; **Result from the post-layout simulation)

smaller nonlinearity. Compared to other DPS architectures [4-6], this work achieves the smallest pixel pitch and memory area ratio, which is shown in Fig.7. Finally, with the proposed self-cutoff technique, it consumes only 75.3 µW at the highest achieved frame rate of 181.8 fps, resulting in the best imaging figure of merit (iFoM) performance among all works.



(a) (b)

Fig. 7. The (a) chip micrograph along with the (b) pixel layout

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